WHAT IS CLAIMED IS:

1. A method for noise management in a mixed signal processor integrated circuit having a digital processing section and an analog section, comprising the steps of:

clocking the digital processing section at a first clock rate; and

inhibiting clocking of the digital processing section during at least a portion of a data conversion operation by the analog section to prevent noise from clock transitions in the digital processing section from being injected into the analog section during the at least a portion of th data conversion operation.

2. The method of Claim 1, wherein the step of inhibiting is initiated in response to a request signal from the analog section prior to performing the at least a portion of the dat a conversion operation.

3. The method of Claim 3, wherein the analog section initiates the data conversion operation in response to a request for a data conversion operation generated by the digital processing section.

4. The method of Claim 1, wherein the step of inhibiting is operable to decrease the clock rate of the digital processing section.

5. The method of Claim 4, wherein the data conversion operation occurs within less than a cycle of the clock operating the digital processing section.

6. The method of Claim 1, wherein the step of inhibiting operates during substantially the entire data conversion operation.

7. The method of Claim 1, wherein the step of inhibiting is in response to a signal generated by the digital processing section.

8. The method of Claim 7, wherein the step of inhibiting requires a handshake between the digital processing section and the analog processing section, such that there will be a signal required

from the analog processing section to the digital processing section prior to the step of inhibiting being operable.